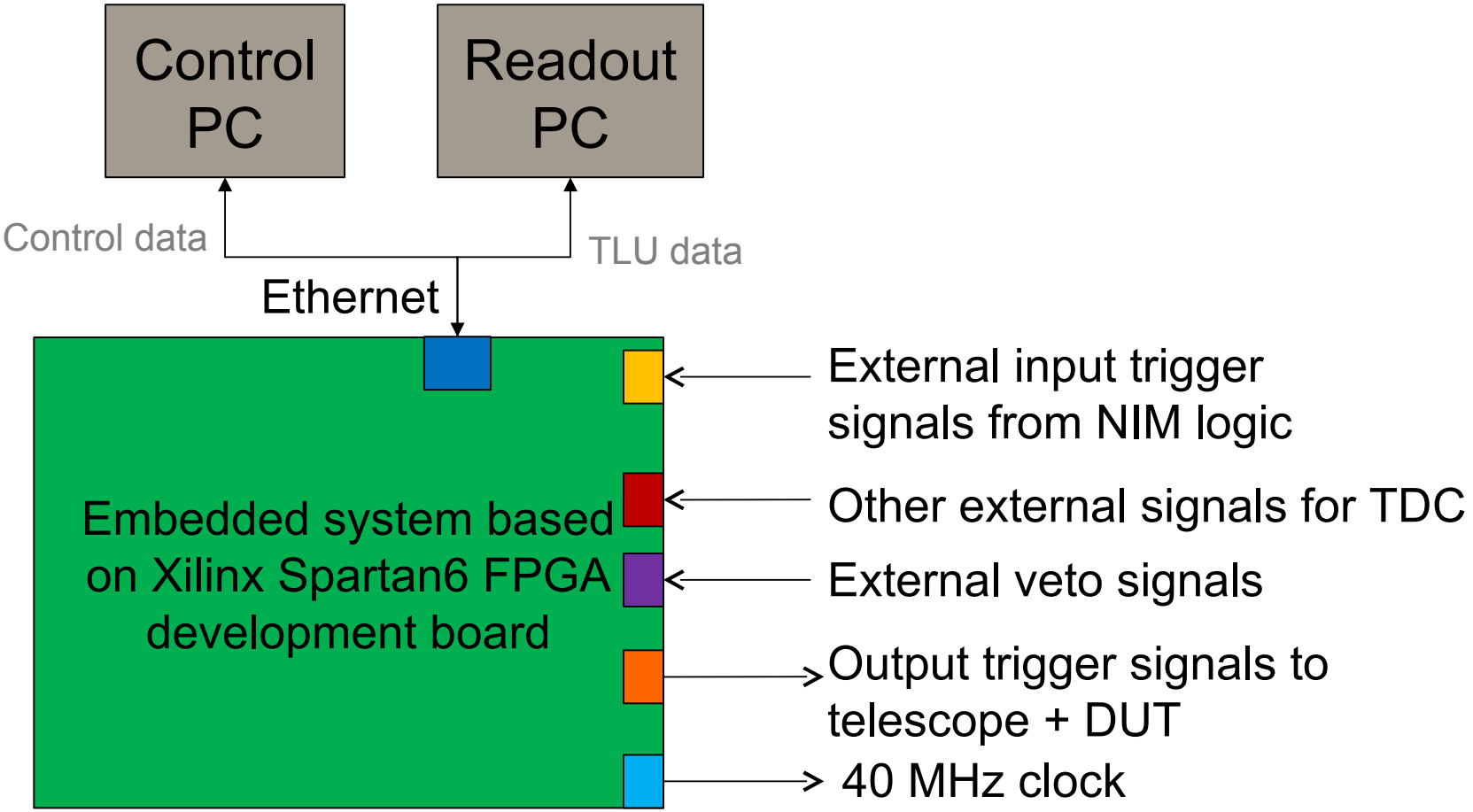
TLU plans

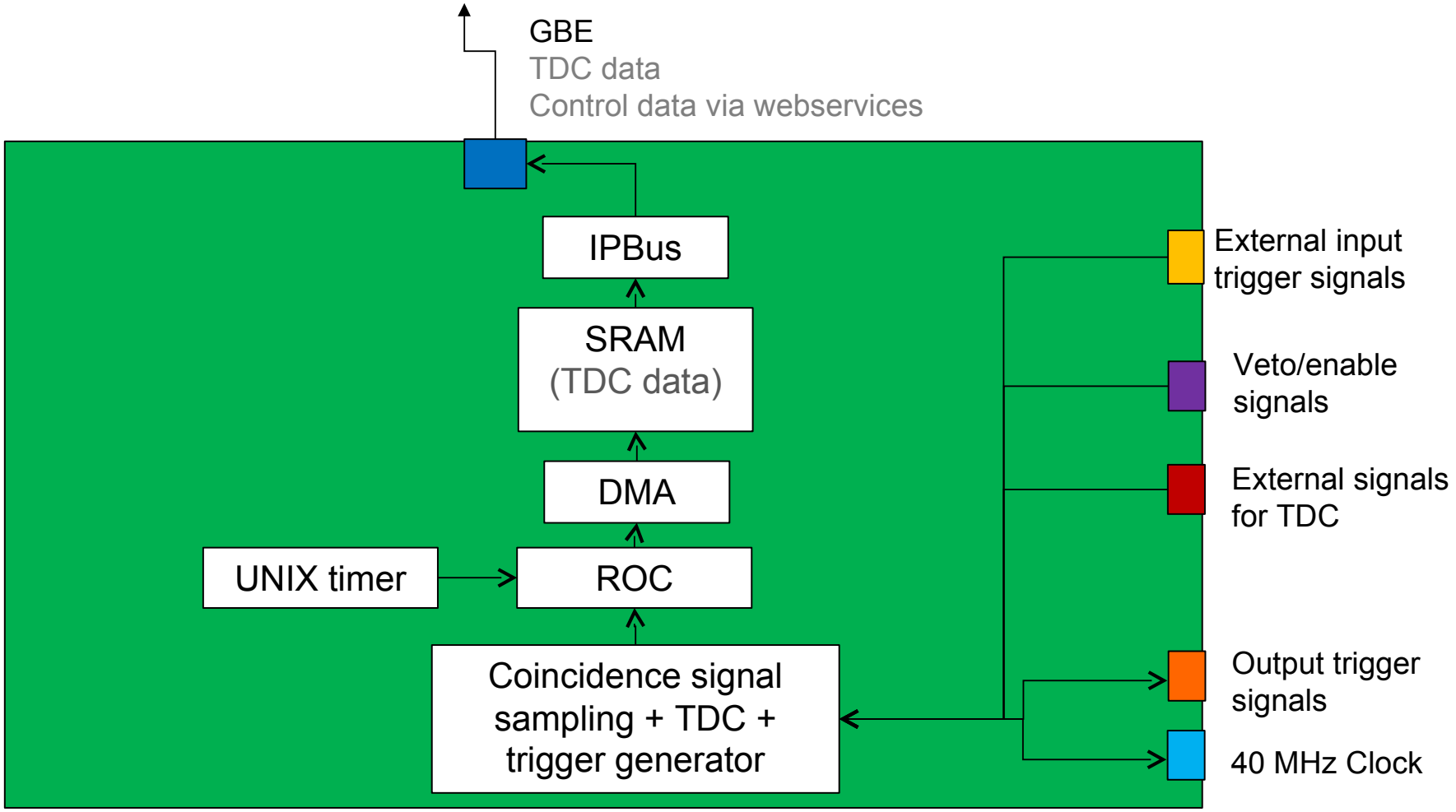
Motivation

- Have a compact trigger logic unit in one board instead of tens of VME modules and lemo cables dangling around.
- Easy configuration of trigger logic remotely with added functionalities such as test readout elements (TimePix + DUT) without beam (ie auto trigger).
- Make the logic a bit generic such it can be attached to LHC like read-out systems.
- Implement a TDC that provides timing information.

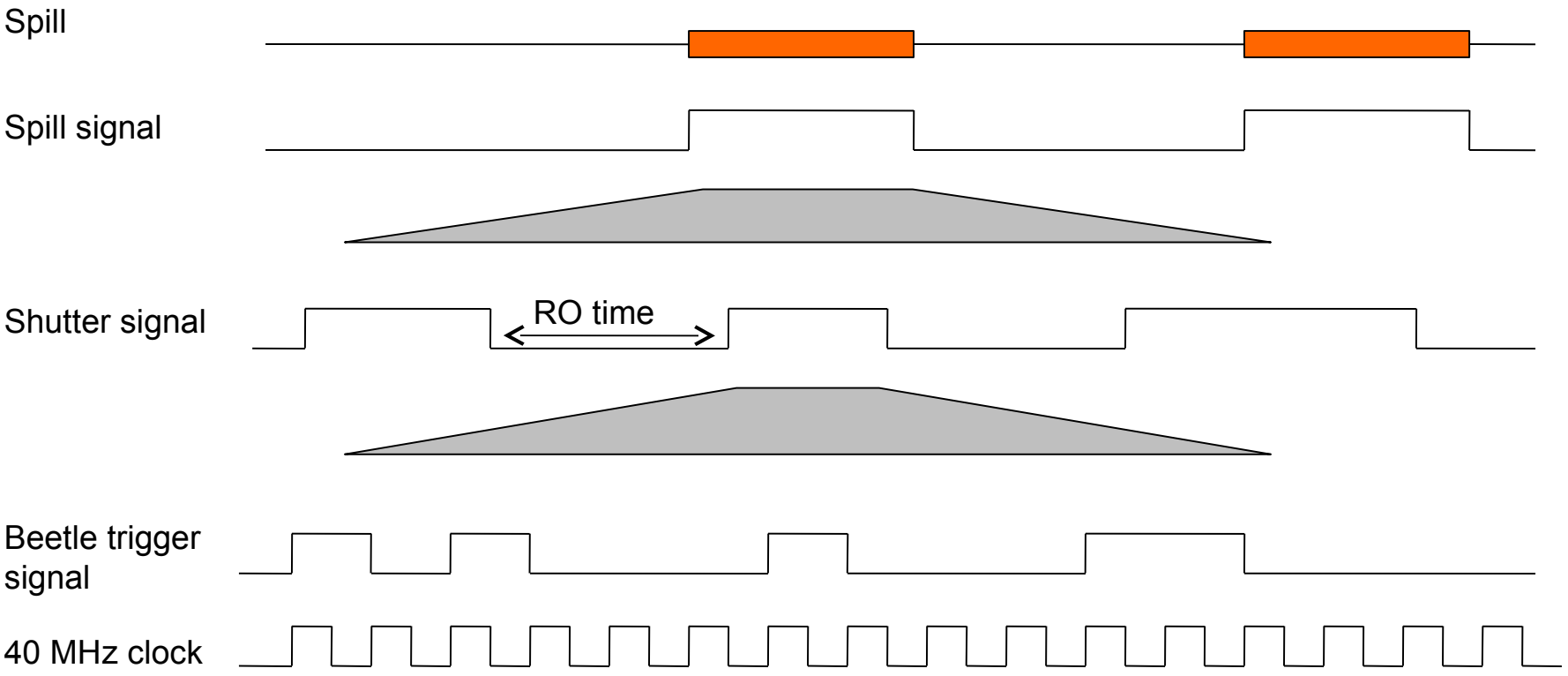
General scheme (1)



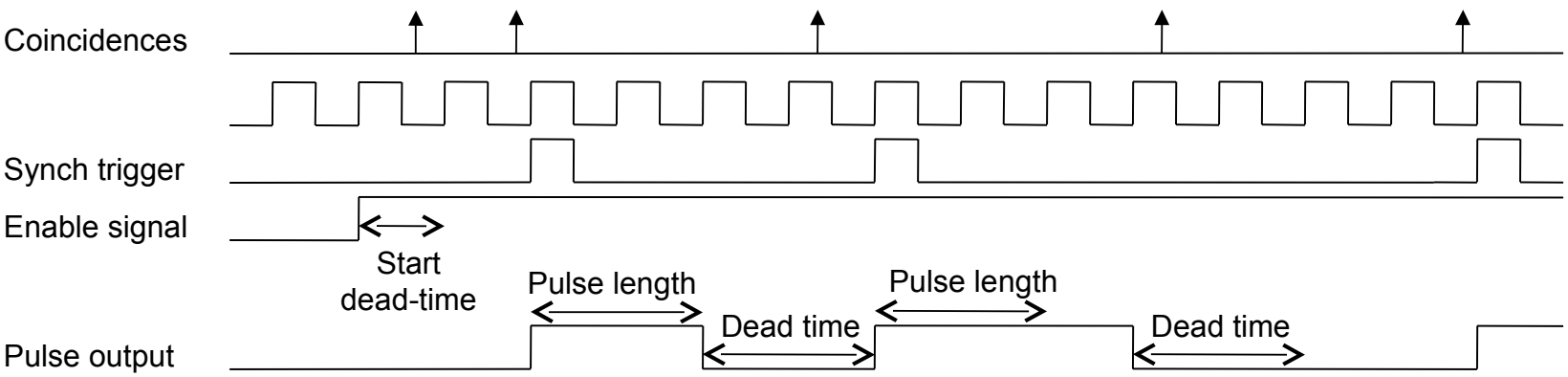
General scheme (2)



Signaling example



GPP: General Purpose Pulser



General purpose pulser (GPP)

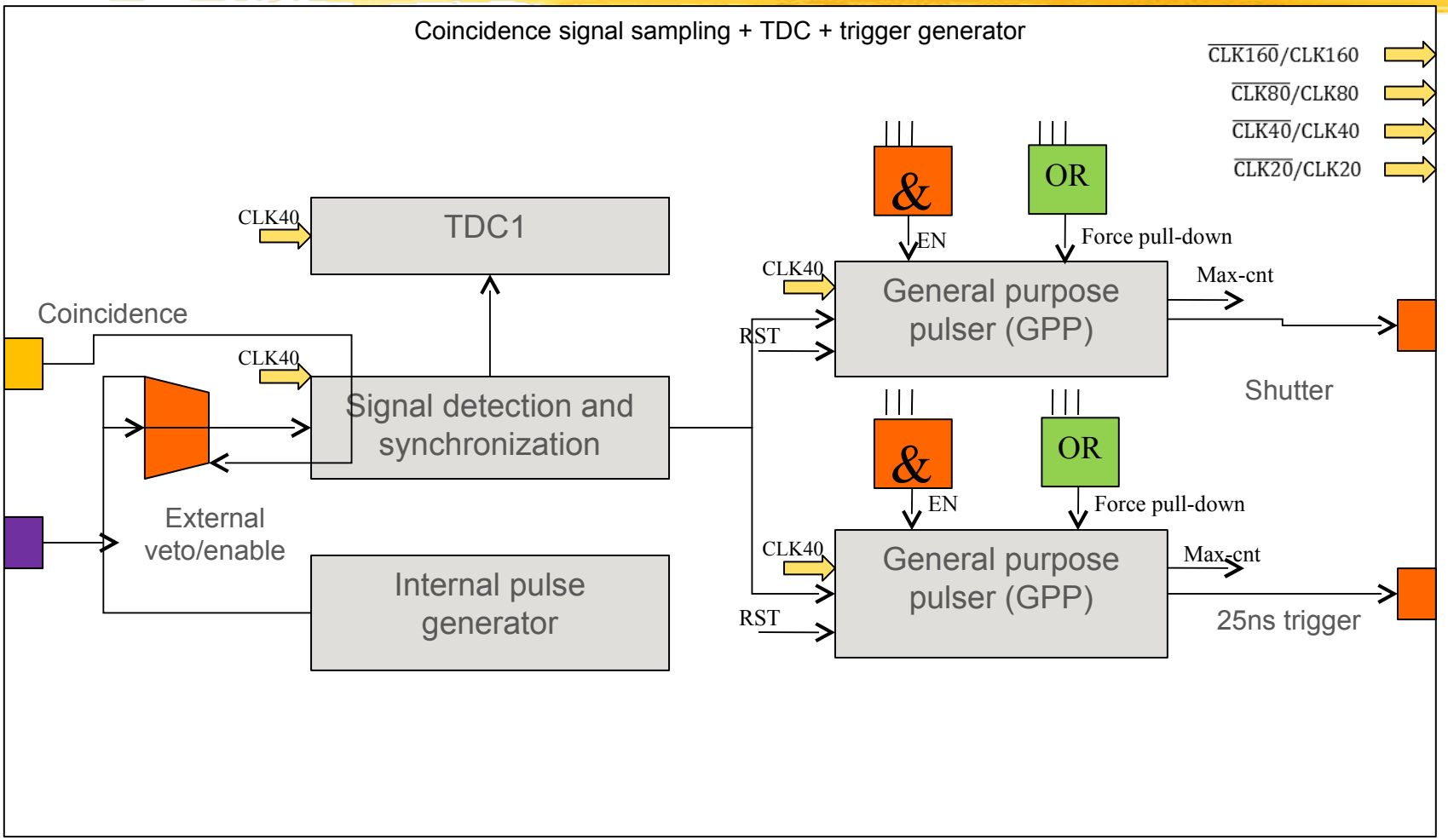
Programmable features:

- Startup dead time.
- Pulse length.
- Inter-pulse dead-time.
- Max pulse count.
- Output delay in clock cycles.
- With updating or non-updating.
- Enable/veto with programmable coincidence input to select several sources.
- Force cero input with programmable OR input to select several sources.

GPP 2

- Using several GPPs with multiplexor at the enable/veto and "force-pull down" inputs we can implement the different output signals:
  - Spill signal:
    - Long pulse length.
    - With updating.
  - Timepix shutter signal:
    - Pulse length modulated by external "force '0' output".
    - Dead time = timepix readout time.
  - Beetle trigger signal:
    - Pulse length = '1'.
    - Dead time = '0'.
    - Max counter.
  - Veto/enable multiplexors:
    - The Spill signal enables the "Timepix shutter" and the "Beetle trigger" signals.
    - The "Beetle trigger" max counter forces the pull-down of the "Timepix shutter".

Internal scheme (1)



The TDC ('s)

TDC

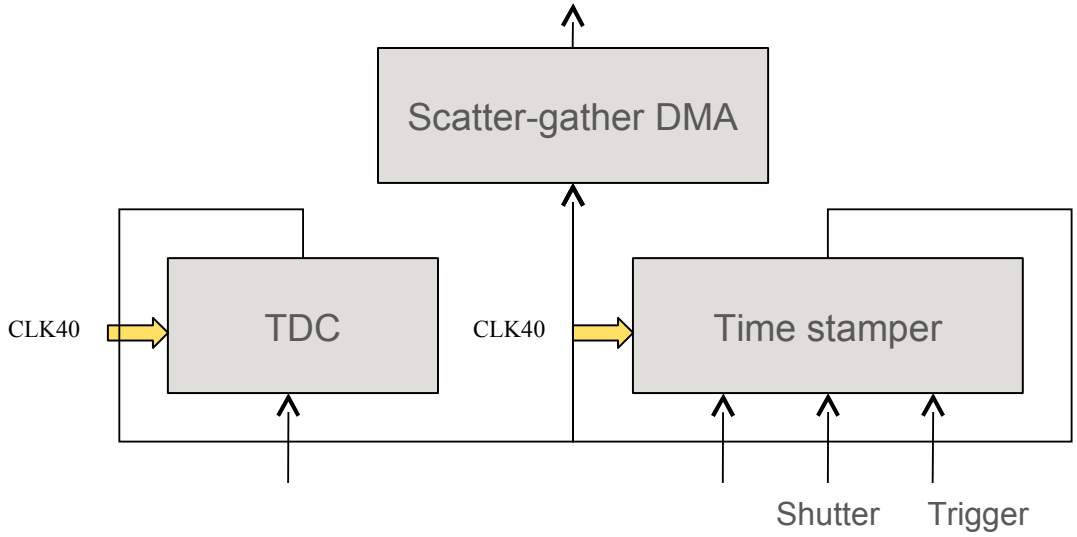
Features:

Implementation based on ISERDES, Deserializer/Serial-to-Parallel Converter. Precision of 1ns.

- Output data format to be defined.
- Some extra bits with extra status info. To be defined.
- The scheme also defines the signal synchronization circuitry.

Time stamping of output signals

- It may be helpful to record the time when a transition in any of the output signals ocurred. Two options:
  - A TDC per output signal. Too heavy.
  - Have a clock counter and use it as time stamp.



Other technical issues

- In this first design make something simple that works:
  - All clocks synchronous.
  - Will not use fancy improvements in the logic which would increase the data Tx rate.
- Later improvements:
  - Think about an architecture that permits the TDC and the pulsers work in different clock domains so an external input clock could be used to generate the trigger signal while keeping the TDC untouched.
  - Zero-suppression…

Other technical issues

- NIM voltage levels compatibility:
  - Use LVPECL or build a small adapter board.
  - In the future, maybe we could build a plug-in board with the discriminators and coincidence units.
- Output data format:
  - To be defined.
- Software development needed:
  - Firmware for the embedded system.
  - TLU reader: the Rx software at the readout PC.
  - TLU controller: webservices based control (html page).

Status

- Ethernet link working and GBE implemented with IPBus.
- VHDL for the pulser ready.
- Working in the TDC using ISERDES
- Working in the assembling of the parts.