The LHCb VELO upgrade


a CERN, European Organisation of Nuclear Research, Geneva CH1211, Switzerland
b Friedrich-Alexander-Universitaet Erlangen-Neurnberg, Schlossplatz 4, 91054 Erlangen, Germany
c Department of Physics and Astronomy, Kelvin Building, University of Glasgow, Glasgow G12 8QQ, UK
d Department of Physics, University of Liverpool, Liverpool L69 3BX, UK
e Nikhef, Science Park 105, 1098 XG Amsterdam, The Netherlands
f The Denys Wilkinson Building, Keble Road, Oxford OX1 3RH, UK
g Instituto de Fisica - UFRJ, Cidade Universitaria, CP 68528, 21941-972 Rio de Janeiro - RJ, Brazil
h University of Santiago de Compostela, 15782 Galicia, Spain
i Stockholm University, SE-106 91 Stockholm, Sweden
j Syracuse University, Syracuse, NY 13244, USA
k Department of Physics, University of Warwick, Coventry CV4 7AL, UK

Abstract

The LHCb experiment at the LHC plans to massively increase its data taking capabilities by running at a higher luminosity with a fully upgraded detector around 2016. This scheme is independent of (but compatible with) the plans for the SLHC upgrades. The silicon detector will be upgraded to provide a 40 MHz readout and to be able to cope with the increased radiation environment. This paper describes the options currently under consideration. A highlight of the R&D so far undertaken is a beam test during summer 2009 using the Timepix chip to track charged particles. Preliminary results are presented, including a measurement of the resolution achieved by the 55 \( \mu \text{m} \) pitch pixel array of better than 9 \( \mu \text{m} \) for perpendicular tracks and 55 \( \mu \text{m} \) for angled tracks.

1. Introduction to the LHCb Upgrade

LHCb [1] is an experiment installed at one of the four collision points of the Large Hadron Collider (LHC). It is dedicated to the search for New Physics via the reconstruction of the enormous flux of beauty and charmed hadrons expected at the collider. This data sample will be used to make precision measurements of CP violation and to search for rare decays. The physics reach of the experiment is largely due to the expected \( \approx 500 \mu \text{b} \) production cross-section of B hadrons at 14 TeV centre of mass energy proton collisions, together with the fact that all species of B-hadrons are produced, in particular \( B_s \). The detector is laid out as a single arm spectrometer between an inner square acceptance of 15 mrad and an outer rectangular acceptance of \( 250 \times 300 \text{mrad} \), and is designed to trigger on and optimise the acceptance for \( B \bar{B} \) production, which is correlated and sharply peaked in the forward-backward direction. Due to the possibility to tune the \( B \bar{B} \) at the LHCb interaction point, the experiment can be run at a luminosity of choice, and LHCb expects that after the LHC commissioning period, the design running luminosity of \( 2 \times 10^{32} \text{cm}^{-2} \text{s}^{-1} \) will be comfortably reached. During the initial running phase, when LHCb expects to accumulate \( 10 \text{fb}^{-1} \) over a period of about 5 years, key measurements will include a first observation of the rare decay \( B_s \to \mu^+ \mu^- \), a measurement of the mixing phase in \( B_s \to J/\psi \phi \) at the level of the SM prediction, and the first precise measurements of the CKM angle \( \gamma \) via a large number of decay modes [2].

The flavour sector is expected to be a sensitive probe for New Physics. This might be directly discovered at LHCb during the first phase of operation, or there will be precise flavour sector measurements needed to further elucidate any NP discoveries at the general purpose detectors ATLAS and CMS. For these reasons, together with the fact that after the accumulation of the initial dataset the statistical improvements that can be expected while...
2. Upgrade design issues for the LHCb vertex locator (VELO)

2.1. Introduction

A detailed description of the current LHCb VErtex LOcator (VELO) design can be found in Ref. [3]. A key feature of the design is two retractable detector halves each housing 21 R and $\phi$ measuring silicon modules. Each half operates in a vacuum, separated from the LHC primary vacuum by a 300 $\mu$m thin aluminum foil, which serves as a wakefield guide for the LHC beams. During LHC injection the halves are retracted by about 30 mm from the beams, and when stable collisions are established the halves can be centred, so that the innermost strips of the $R$ measuring sensors form a circle around the collision point with a radius of about 8 mm. Each module contains an individual $R$ and $\phi$ measuring sensor, with pitches which vary with radius, starting at about 40 $\mu$m at the innermost region. The sensors are manufactured with n-on-n strips in diffusion oxygenated float zone silicon, which at the time of manufacture was the most appropriate radiation hard solution. The approach of the closest sensitive point to the beam is limited by the need for a guard ring of about 1 mm, a 1 mm tolerance to the foil, plus the thickness and tolerance of the foil itself. The intrusion of the electronics in the acceptance is limited by placing the chips around the outside of the silicon, and routing the signals out via a double metal layer. The upgraded VELO is expected to keep the concept of retractable detector halves, but the silicon modules and the foil will be completely redesigned and replaced according to the design issues outlined below.

2.2. Irradiation issues

The current VELO is designed to withstand an integrated luminosity of about 10 fb$^{-1}$. After this time the signal to noise is expected to drop, and the current temperature drop of about 19 °C between the CO$_2$ cooling channel and the silicon tip is expected to be insufficient to protect the module from going into thermal runaway. Operating to the end of the lifetime of the upgrade will result in a total flux of about $0.8 \times 10^{16}$ n$_{eq}$ cm$^{-2}$, and in the case of a pixel chip with the electronics in the acceptance, this would be equivalent to a total ionising dose of about 370 Mrad. After this dose, we would expect currents of approximately 300 $\mu$A/cm$^2$ at $-15$ °C at a bias voltage of 900 V at the innermost radius. For short strips similar to the current design this would give a current of 1–2 $\mu$A, and roughly 10 nA for $55 \times 55 \mu$m$^2$ square pixels [4]. At these doses and currents, the most challenging issue will be protecting the silicon tip from thermal runaway, without introducing too much material into the acceptance.

2.3. Geometry issues

The trigger algorithms of LHCb in both the current detector and the upgrade rely on an impact parameter cut, hence the impact parameter resolution is an excellent benchmark performance number for the detector. The global constraint on the detector construction is the $\approx 1.2$m length of the vacuum tank. From our previous studies [5] we know that the impact parameter resolution is well-described to first order by the following expression:

$$\sigma_y = \frac{r_2}{p_T} \sqrt{2 \times 0.0136 \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln \left(\frac{x}{X_0}\right)\right)^2 + \frac{A_{0x}^2 \sigma_y^2 + A_{0x}^2 \sigma_x^2}{A_{12}^2}}.$$

In this formula $r_2$ is the radius of the first measured point, $p_T$ is the transverse momentum of the track, $x/X_0$ is the fractional radiation length before the second measured point, which includes the foil, any dead area of silicon traversed, and the material of the first measured point, $\sigma_x$ and $\sigma_y$ are the measurement errors on the first and second point, respectively, and $A_{0x}$ represents the distance between $x$ and $y$, where $x$ and $y$ can be 0 (the interaction region), 1 (the first measured point), or 2 (the second measured point). This formula gives an indication of the driving factors behind the design. The presence of the $p_T$ term indicates that the first measured point should be as close to the interaction point as possible. This is achieved by aiming for the minimum possible inner dimensions, and by having as many stations as possible such that the extrapolation distance of the low angled tracks is minimised. It is also helpful to use sensors with a minimum of dead region at the inner edge coming from the guard ring. It should, however, be borne in mind that as the inner dimension is reduced, the irradiation levels rise quadratically, and the design must deliver sufficient cooling to this region to avoid thermal runaway. As an indication, the radius of the first measured point for a typical track distribution in LHCb, emerging from an interaction vertex with a width in $z$ of about 6 cm is illustrated in Fig. 1, for the current layout of 21 stations, and for the case that 10 stations would be removed. The presence of the $\sqrt{x/X_0}$ term shows on the other hand, the importance of reducing the number of stations, of having the stations as thin as possible, and of reducing if possible the material contribution of the RF foil which encapsulates the detector secondary vacuum volume. The impact of this material term on the impact parameter resolution as a function of transverse momentum is illustrated in Fig. 1. The final term in expression in Section 2.3 illustrates the importance, for high momentum tracks, of keeping the precision as good as possible. There are additional considerations which enter into the
design, in particular, the importance of having stations surrounding the interaction region on both sides, in order to measure the primary vertices as accurately as possible, and the overall performance of the detector in terms of the trigger algorithm and the time taken to implement this algorithm in the computer farm.

2.4. Data rates

Imposing a 40 MHz readout results in a huge data rate output needed from the front end chip, with the number of particle hits per crossing reaching $\approx 5 \times r^{-1.9}$ at the highest luminosity, where $r$ is the radius in cm. Taking the model of a $256 \times 256$ matrix pixel detector (as outlined in the following sections), and assuming an average cluster size of 2 leads to the conclusion that from the innermost chip the data rate would be 10.9 Gbit/s and a total data rate of 2700 Gbit/s for the entire detector. This would require a minimum of 840 data links running at 3.2 Gbit/s. On top of this, extracting the data from the pixel matrix to the pixel periphery becomes non-negligible at these rates and a fundamental design change is needed for the front end chip.

3. Strip solution

3.1. Introduction

If the problems of radiation hardness and thermal runaway can be overcome, a strip detector with finer segmentation and an appropriate readout chip remains an option for the VELO upgrade. For such a design to proceed, confidence is needed that the pattern recognition performance and the time needed for the triggering algorithms can satisfy the LHCb requirements; if not then a pixel solution will be mandatory (see next section). The basic concept is illustrated in Fig. 2. The module would be double sided, with 200 µm thick $R$ and $\phi$ measuring sensors and the addition of a 200 µm thick diamond plane to drain the heat away from the silicon. Initial thermal studies indicate that with the current CO$_2$ cooling channel temperature of between $-30$° and $-35$° this will be sufficient to cool the tip of the silicon. The baseline upgraded strip design will stay as close as possible to the current design. The following issues are taken as the main inputs for the upgraded design:

![Fig. 1. Figure illustrating some design issues of the LHCb VELO upgrade. The current layout in the x–z view is illustrated in the upper left part of the figure. Below this, the radius of the first measured point is shown for the current design (solid line) and for the case that 10 stations would be removed (dashed line). This plot illustrates the term $r_1$ which appears as equation in Section 2.3. On the right side of the figure various impact parameter resolutions are shown as a function of $1/p_T$ where $p_T$ is the transverse momentum in GeV. The top plot shows what would happen if the amount of material in the individual VELO stations would be increased by a factor 2 or 4. The lower plot shows what would happen in the case that the material in the RF foil could be reduced by a factor 2 or 4.](image1)

![Fig. 2. Possible layout of strip detector module.](image2)
• **Signal to noise ratio (SNR):** The radiation dose expected to be accumulated in the VELO sensors in the upgrade scenario is about $0.8 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ for a total integrated luminosity of 100 fb$^{-1}$. According to the latest estimates [6] it should be possible to observe a signal of around 8000 electrons after such a dose, if the appropriate annealing scenario is applied. The current developed in the sensor will, however, require an improved cooling delivery to the sensor tip, to avoid thermal runaway. An example of the kind of improved cooling delivery to the sensor tip, to avoid thermal current developed in the sensor will, however, require an improvement.

• **Number of channels:** The current design of signal routing in the VELO sensors brings a considerable complication in terms of clustering and common mode suppression in the TELL1 FPGA algorithms. For the upgrade, where the chip may have to include a common mode suppression capability, this should be improved. The routing should therefore be improved to group together signals from the same part of the detector. In addition, for the R detector, the routing should minimise the capacitance for the most irradiated strips, where the signal loss is expected to be greatest.

• **Sensor size:** A rectangular shape can bring an advantage in capacitive load, as well as better matching the rectangular acceptance of LHCb. If the current 3 cm spacing along the beam axis is maintained for the closely packed modules, then external dimensions of 35 mm × 30 mm seem reasonable.

• **Number of channels:** Increasing the number of channels can bring an advantage in terms of occupancy. With the dimensions given above, there is space to fit 20 ASICs around the sensor (the current die size is 5.1 mm along the short edge). The dimensions of a future chip will be further optimised, as the use of 130 nm technology and the removal of the analog pipeline will bring significant space savings, although the extra features needed in the chip such as analog to digital converters and on-chip common mode suppression must also be accounted for. As an additional benefit, the removal of the intermediate pitch adapter will bring a gain in SNR.

• **Minimum strip pitch:** Reducing the minimum strip pitch should be possible with the latest advances in via technology. This will be necessary to increase the channel count, as well as bringing the advantage of a more precise measurement for the first point on the track, which is important for the impact parameter resolution. It should also be noted that it is expected that after heavy irradiation the resolution will not be significantly better than binary, in which case a smaller minimum pitch is also helpful. The total resistance presented to the electronics front end must also be controlled, from an SNR point of view.

• **Minimum radius of first measured point:** Reducing the radius of the first measured point will improve the multiple scattering term component of the impact parameter resolution, by about 10% per 0.5 mm reduction. From studies performed for ATLAS [8] it seems that a guard ring width of 0.5 mm is possible, which would allow a minimum first measured radius of 7.5 mm, within the physical constraints of the current RF foil.

• **Occupancy:** The occupancy in minimum bias events is expected to go up by roughly a factor 2.9, for an increase of 10 in luminosity, assuming that with full knowledge of every event there is no cross talk from the previous or next beam crossing. For signal events the occupancy increase is about 2.5. The occupancy distribution within the sensor can be further improved by increasing the number of strips, as discussed above, and by matching the strip pitch precisely to the particle occupancy as a function of radius. Preliminary studies show that at the upgrade the occupancy can be brought below 1%, for operation at the highest luminosity.

• **Detector signal routing:** The current design of signal routing in the $\phi$ sensors brings a considerable complication in terms of clustering and common mode suppression in the TELL1 FPGA algorithms. For the upgrade, where the chip may have to include a common mode suppression capability, this should be improved. The routing should therefore be improved to group together signals from the same part of the detector. In addition, for the R detector, the routing should minimise the capacitance for the most irradiated strips, where the signal loss is expected to be greatest.

There are four main changes envisaged. The silicon will be reduced in size slightly, in order to be able to better match the $300 \times 250 \text{ mm}^2$ angular acceptance of LHCb, while minimising the distance to the readout chips and hence the capacitive load. The total number of strips will be increased to 2560 (corresponding to 20 chips, each with 128 readout channels, of the current 16 chips). The minimum pitch will be decreased from the current 40 to 25 or 30 $\mu$m, and the first sensitive strip will be placed slightly closer to the interaction point. The double metal layer routing of the $\phi$ detector will be improved to eliminate the current scrambling of channels corresponding to different regions of the detector in the readout chip, which will ease the problem of on-chip common mode suppression. The occupancies which can be achieved with such a design are very reasonable, as illustrated in Fig. 3.

The manufacture of first prototypes to demonstrate the feasibility of this design is planned to be carried out in 2010. For radiation resistance it is mandatory to use $n$ strips, which can be achieved using a single sided process and $n$-in-$p$ technology. The main challenges will lie in obtaining the minimum possible strip pitch, verifying the radiation resistance and implementing the complex double metal routing. The development of the ASIC will proceed in synergy with the other sub-detectors of LHCb which require such a chip.

4. **Pixel solution**

4.1. **Introduction**

A second option for the upgrade is to change the readout concept from a strip to a pixel readout, which brings potential advantages in pattern recognition capabilities for the trigger. The VELO group is currently performing R&D to demonstrate the feasibility of such a solution, and initial investigations have focused on a derivative of the Medipix/Timex family of chips as a candidate for the FE electronics. In the following section we discuss this chip, and give preliminary results from a test beam which was performed in Summer 2009 to demonstrate the feasibility of using this chip for charged particle tracking. We discuss here a solution using planar silicon as the sensing element; however, the concept of using diamond or 3D silicon detectors are also being considered.

4.2. **Timex overview**

The Timepix [9] is a pixel readout chip, based on its predecessor the Medipix2. There are 256 × 256 pixels of 55 $\mu$m by 55 $\mu$m square and the overall dimensions of the chip are 14 mm × 14 mm. The chip is three side buttable with on one side a dead region containing the peripheral circuitry and bonding pads of 1.8 mm. This can be further reduced to 0.8 mm by removing the bonding pads and using TSV’s (through silicon vias) to provide I/O connectivity through the back of the die. The analog power consumption is around 400 mW, i.e. 6 $\mu$W per pixel. The digital power is another 400 mW, running at 40 MHz. Each pixel digitizes the charge by measuring the TOT.
The chip would have to be modified to be appropriate for a Velopix application and a design cycle is planned for 2009/2010. The current Timepix is a multipurpose chip, and in this design cycle a Velopix derivative can be optimised, discarding the features of the architecture which are not needed, and adding those specific to the VELO. The main features of the Timepix which make it potentially attractive for the VELO upgrade are:

- **Square pixel size**: The default Timepix pitch of $55 \times 55 \, \mu m^2$ allows a measurement with adequate precision simultaneously in the both $x$ and $y$ projections. This allows us to construct single sided pixel modules, with the corresponding material budget advantage.
- **Front-end pulse shape**: The Timepix pulse shape has a rise time of 90 ns and a fall time tuneable down to 500 ns. This will give negligible loss given the expected maximum occupancies of around 0.02%.
- **Leakage current**: The chip is already constructed to tolerate a leakage current of around 10 nA per pixel, which corresponds to the range expected for the most irradiated parts of the detector at the end of the running period.
- **Dimensions**: The very small chip periphery should make it possible to construct a tiled sheet of chips with no loss in coverage. Elongated pixels of 800 $\mu m$ can cover the dead spaces between the chips. The use of edgeless sensors should allow a close approach to the beam.
- **Technology**: The Timepix is currently built in 0.25 $\mu m$ technology, which is very advantageous from the point of view of power consumption and radiation hardness. An upgrade to 130 nm, corresponding to what has been implemented for Medipix3 is forseen for the next Timepix design cycle, which will again to improve these features. The dedicated VELO ASIC, which is very close to the Timepix architecture, will benefit from such an upgrade.
- **Radiation hardness**: New irradiation results from the Medipix3 chip show that integrated doses of 500 Mrad are within reach [10]. These results are very encouraging for a future...
Timepix application and correspond to the radiation tolerance required.

- Potential for synergy with other elements of the LHCb upgrade programme: A possible choice for the upgrade of the RICH component of LHCb would use a new HPD based photodetector system. In this case a pixel detector chip must be realised, preferably in 130nm technology, capable of a 40MHz sustained readout rate. In this case the first steps towards chip development would be taken in common with the VELO, with an eventual splitting at the final step for the different requirements.

5. Baseline pixel layout

If the current mechanics are kept, the modules must be constructed and laid out within a total width of about 20 cm, and cannot be placed further than 750 mm downstream from the interaction point. The baseline layout remains similar to the currently installed VELO layout, with U-shaped stations which fit around the RF foil in its current shape. Each station consists of 10 ASICs bump bonded onto three pieces of silicon in a compromise between reducing the dead space due to the guard rings, and optimising the yield. The cooling is provided by a diamond plane, which can also be metallised in order to route signals. The active area is maintained under the chip periphery by elongating the pixels in this region to dimensions of $800 \times 55 \mu m^2$. Initial thermal studies show that if the current bi-phase CO2 system is used, it should be possible to achieve a temperature difference of under 5°C at the tip of the module, with a 200 µm thick diamond plane, assuming a thermal conductivity of 1600 W/m K [11]. In this layout the closest pixel to the beam line lies at 7 mm, with the pixels around the square corners of the hole being further away. The baseline module design is illustrated in Fig. 4. The layout has been investigated with a toy Monte Carlo which generates tracks flat in eta in the LHCb acceptance and originating from a vertex at $z = 0$ with a width of 5.3 cm. The number of tracks with three hits or more, in such a configuration is 99.89%, which compares well to the 99.94% of the current VELO. The diamond and silicon layers contribute 0.6% of a radiation length, and if the extra contribution of the metallisation layers and power tapes can be engineered to not add significantly to this the material contribution of the modules will be comparable to the current VELO.

5.1. Timepix modifications

The current version of the Timepix chip, which is based on the medical imaging shutter concept of the Medipix chip, is in appropriate for the LHCb upgrade and significant changes will be needed to render its capable of continuous, dead-timeless operation at 40MHz. A novel architecture compatible with the small pixel size will be required to allow the fast processing and transmission of data, and this must be achieved while keeping the power consumption at a minimum. The pixel functionality will be changed to add time-stamps to the hits, and the time-over-threshold count range and resolution can be reduced to be compatible with the expected silicon signal; 4–6 bits is expected to be sufficient. The design of the digital, analog, and data buffering parts are planned for the next design cycle of the Timepix chip during 2010. The new ASIC will be implemented in the 130 nm technology, similarly to the Medipix3 chip. It will require testing for radiation hardness, single-event upset rates, and compatibility with the LHCb VELO sensor candidates.

An important example of the type of parameter which must be controlled is the timewalk. Small signals which are just above threshold, which can occur due to charge sharing in multi-pixel clusters can be assigned to the wrong bunch crossing, resulting in splitting of clusters between events, and the possible formation of “ghost” tracks. The problem is accentuated at high luminosity, where more of the bunch crossings are filled, and there is an increased possibility of cross talk from neighbouring interactions. This problem can be attacked by introducing positive feedback in the discriminator circuit, and a detailed simulation of the preamp and discriminator combination will be necessary to determine the necessary peaking time to keep the full range timewalk below 25ns. It may also be necessary to introduce local clustering to regroup candidate multi-pixel clusters. Local clustering will also be necessary to keep the data rates at acceptable levels, by allowing the possibility of assigning a single time stamp to a cluster, rather than the individual pixel hits.

Fig. 4. Baseline layout of VELOpix module.
5.2. Data rates

The data rates expected from the modules are an essential parameter of the design. The number of particles which can be expected at the highest luminosity has been calculated [12] to be about 5 \times r^{-1.9} particles per cm$^2$ per bunch crossing, averaged over all sensors in $z$. This gives an estimate of the number of particle hits per event per chip peaking at around 5, as shown in Fig. 5. Initial studies of a fast column readout scheme indicate that the data size will be in the range of (17+22n) bits per cluster of $n$ pixels. The average cluster size will depend on the sensor thickness and will evolve as a function of irradiation. It also depends strongly on the track angle; in LHCb the reconstructable tracks have angles relative to the $z$ axis of between 15 and 300 mrad, with a mean value of approximately 90 mrad. A reasonable initial value for the average cluster size for 150 $\mu$m thickness silicon is expected to be about 2. This gives a maximum data rate of approximately 11 Gbit/s from the most active chip, as illustrated in Fig. 5. The effects of secondaries and delta rays should also be evaluated. The chip must be modified to cope with such an output rate. A development could follow the line of the Medipix3 chip, which has 10 high speed LVDS links at 500 Mbit/s consuming 11 mW per link. Use of the GBT link [13], providing 3.2 Gbit/s would mean that the full VELO system of 42 modules could be implemented with 840 data links.

6. Test beam

During the summer of 2009, a test beam was set up to demonstrate the suitability of the Timepix as a readout IC for a charged particle tracking device. A telescope was constructed with six planes inclined at a double angle (rotated about the vertical axis and the horizontal axis perpendicular to the beam) of 9°. The Device Under Test (DUT) was mounted in the centre of the telescope, with the precise position and angle under remote control via a stepper motor. The telescope was made up of two Medipix and four Timepix planes, with the DUT being a Timepix plane. In each plane the ASIC was bump bonded to a 300 $\mu$m thick p-on-n silicon pixel sensor, biased to 100 V. The assemblies were all readout using USB driven systems provided by Prague CTU [14] and the Pixelman data acquisition and control software [15]. A photograph of the telescope and DUT installed at the SPS 120 GeV pion beam is shown in Fig. 6. The main parameters varied during the two week data acquisition campaign were the pixel thresholds, the angular orientation of the sensor with respect to the tracks, the bias voltage, and the pixel clock speeds and threshold settings. A typical Landau distribution obtained from signals in the DUT is shown in Fig. 7. We show here some preliminary results.

![Fig. 6. Photograph of assembled telescope and DUT.](image)

![Fig. 5. Figure illustrating, for the baseline layout, the average particle rates per bunch crossing (upper number) and the corresponding data rates in Cbit/s (lower number) per chip, at the highest expected operational luminosity of $20 \times 10^{30}$ cm$^{-2}$ s$^{-1}$.](image)

![Fig. 7. Typical distribution of cluster TOT values in the Timepix DUT.](image)
6.1. Cluster size as a function of angle

As discussed above, the cluster size as a function of incident track angle is an important input to the chip design, and affects the occupancies and total data rates from the detector. This was investigated by varying the angle presented by the DUT to the beam between $\pm 18^\circ$. By symmetry, the nominal perpendicular position was determined to be in fact at an angle of $0.22^\circ$. The cluster sizes in the DUT for a threshold of 1000 electrons and for three different angles, are illustrated in Fig. 8. The mean value varies between 1.8 for perpendicular tracks and 3.2 for the most angled tracks. The variation of the mean and rms of the total cluster sizes and the projections in the directions perpendicular to and parallel to the angle of rotation are presented in Fig. 8.

6.2. Resolution as a function of angle

Tracks were formed in the telescope by looking at correlated hits between the planes and an alignment was performed by minimising the $\chi^2$ of the track residuals. A dedicated alignment study was also performed using tracks with large angles relative to the beam direction in order to further constrain the weak...
alignment modes. The positions of the clusters were initially determined by using the weighted centre of the deposited charge. This estimate was further improved by using an “η correction” to linearise the relationship between the position and the weighted charge. The tracks are reconstructed using only clusters in the telescope, and after this analysis, the predicted position of the track at the DUT is known to better than 2.5µm, which is largely sufficient to probe the performance of the DUT itself. Fig. 9 shows the width of the residuals between the tracks and the DUT clusters, as a function of angle. For perpendicular tracks, the width is 9.5µm, dropping to a best value of 5.5µm for tracks angled at 9.5°. The true resolution of the DUT can be estimated by subtracting from these numbers the 2.5µm contribution of the telescope tracks in quadrature. These performance figures are preliminary but already indicate that the Timepix assembly is giving an accurate Landau distribution and a very satisfactory resolution performance. Further improvements can be expected as the telescope alignment is refined, and corrections such as the individual pixel gain correction are included.

6.3. Further analyses

In addition to the preliminary results presented here, further analyses are underway. These include an investigation of the resolution as a function of threshold, number of bits used, and two dimensional rotation, studies of the efficiency, noise and pulse shape, and a comparison of the time walk behaviour with that expected from the chip design. In addition, a 3d sensor was installed in the test beam, bonded to a Timepix chip, and the performance of this device will be compared to the planar sensor described here.

7. Conclusions

R&D for the LHCb VELO upgrade has been presented. The use of a derivative of the Timepix chip as the electronics for the upgrade has been shown to be promising, with a first test beam demonstrating the suitability of this chip, when bump bonded to a silicon sensor, as a charged particle tracking device. A best resolution of 5µm has been achieved for angled tracks.

References